Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THOMAS J. HOLMAN and ANDREW V. ANDERSON

Appeal No. 2003-1111
Application No. 09/164,088[1]

ON BRIEF

Before JERRY SMITH, SAADAT, and NAPPI, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-30, which are all of the claims pending in this application.

We reverse.

BACKGROUND

Appellants' invention is directed to a method and apparatus for tracking the state of a page in a memory device which has at least a dependent bank structure. Attribute entries of a page

[1] Application for patent filed September 30, 1998.

contained in a page entry table are updated according to the command and the access information which is generated by an access control circuit in response to a memory access.

Representative independent claim 1 is reproduced below:

1. A method comprising:

creating a page entry table containing attribute entries including at least a dependency code of a page of a memory device, the page entry table storing a state of the page, the memory device having at least a dependence bank structure, the dependence bank structure having at least a sense amplifier that supports more than one bank of memory cells;

processing access information in response to a memory access;

receiving a command from a circuit; and

updating the attribute entries in the page entry table according to the command and the access information.

The Examiner relies on the following references in rejecting the claims:

Narayan	5,781,789	Jul. 14, 1998
Yoshioka et al. (Yoshioka)	5,796,978	Aug. 18, 1998
Barth et al. (Barth)	6,154,821	Nov. 28, 2000 (filed Mar. 10, 1998)

Claims 1-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshioka, Narayan and Barth.

We make reference to the answer (Paper No. 23, mailed November 5, 2002) for the Examiner's reasoning and to the appeal

brief (Paper No. 22, filed September 30, 2002) and to the reply brief, (Paper No. 25, filed January 16, 2003) for Appellants' arguments thereagainst.

OPINION

The Examiner asserts that Yoshioka teaches most of the recited features in claim 1 including "at least one dependent bank structure, by teaching in column 7, line 30, of the register page being dependent upon the software algorithm" (answer, page 3). However, the Examiner identifies the same dependent bank structure having at least a sense amplifier as missing in Yoshioka (answer, page 6). The examiner relies on Narayan for showing store access to a dependent adjacent bank and on Barth for disclosing a sense amplifier to conclude that a skilled artisan would have found obvious to combine with Yoshioka in order "to aid in aligning memory accesses" (id.).

Appellants argue that neither the software replacement algorithm of Yoshioka relates to a memory device with a dependence bank structure nor any part of the reference discloses the claimed dependency code (brief, page 9). Appellants further assert that the proposed combination of the references lacks a proper motivation since the references have no relevance to the issue of tracking the state of a page in a memory device having independence bank structure (brief, page 11). Appellants also

argue that the combination would not have resulted in the claimed structure as the Examiner provides no technical principle for such combination (id.).

In response to Appellants' arguments, the Examiner asserts that the claim merely requires "a dependency code of a page of a memory device" without any correlation between the dependency code and the dependence bank structure (answer, page 8). Furthermore, the Examiner questions the features to which the claimed "dependence" refers to and characterizes the dependence bank structure as an internal structure (answer, page 8) which is similar to Yoshioka's dependence of a memory bank contents on the replacement algorithm used within the bank (answer, page 9).

Appellants respond by arguing that the limitation of "dependency code" is actually recited in the claim and cannot be interpreted to mean something other than what is intended since it has a meaning which is well supported in the disclosure (reply brief, page 4). Appellants further concludes that based on its intended meaning, the claimed "dependency code" and the "SV bit" of Yoshioka cannot be the same (reply brief, page 5).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). To reach a conclusion of

obviousness under § 103, the examiner must produce a factual basis supported by teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Such evidence is required in order to establish a prima facie case. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). The Examiner must not only identify the elements in the prior art, but also show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Initially, we find the fact that the Examiner's position in the statement of the rejection is different from that in the response to arguments section in the answer somewhat concerning. For example, the Examiner's statement of the rejection (answer, page 3) indicates that the dependence bank structure is taught by Yoshioka in column 7 whereas later on page 6 such limitation is identified as missing in Yoshioka. Additionally, instead of setting forth a prima facie case of obviousness, the examiner expands the basis of the rejection in the argument section in an attempt to fit the claims to the prior art teachings, which is neither acceptable nor convincing.

Next, a review of Yoshioka confirms that the reference relates to a data processor with improved address translation method (col. 1, lines 9-12). Although the reference describes the process of replacing missed information from one of the banks (col. 5, lines 31-46), using a replacement software for the bank to be replaced (col. 7, lines 18-30), the disclosed banks are not the same as the claimed dependence bank structure. Therefore, contrary to the Examiner's characterization, we find that the replacement algorithm of Yoshioka is unrelated to a dependence bank structure, as recited in claim 1 and described in Appellants' disclosure. Similarly, we note the Examiner's struggle in reading the claimed "dependency code" on the "SV bit" of Yoshioka by reasoning that "it [SV bit] indicates whether the virtual page depends on single or multiple virtual page support" (answer, page 8). This is not what the skilled artisan would have understood to be the meaning of the claimed "dependency code," as described in the specification.

Narayan and Barth, on the other hand, relate to a mask decoder circuit and initialization of DRAMs, respectively. Although we agree with the Examiner that some kind of memory banks or sense amplifiers are described by these two references, we do not find any specific teaching in either of them that would have been related to the claimed dependency code. Furthermore,

in concluding that Narayan's alleged "aid in aligning memory" (answer, page 6) justifies the combination, the Examiner attempts to forge a combination of unrelated disclosures related to memory addressing, memory initialization methods and a decoder circuit. Thus, even assuming, arguendo, that it would have been obvious to combine Yoshioka with Narayan and Barth, as held by the Examiner, the combination would still fall short of teaching or suggesting the claimed dependency code and the page entry table containing attribute entries that include such dependency code. Accordingly, as the Examiner has failed to set forth a prima facie case of obviousness, we do not sustain the 35 U.S.C. § 103 rejection of claims 1-30 over Yoshioka, Narayan and Barth.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1-30 under 35 U.S.C. § 103 is reversed.

REVERSED

JERRY SMITH Administrative Patent Judge	)
MAHSHID D. SAADAT Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
ROBERT NAPPI Administrative Patent Judge	)

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